IMPROVEMENT IN 3-WEIGHTED PATTERN GENERATION

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ABSTRACT:

Weighted pseudorandom built-in self-test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both less testing time and less consumed power. In this paper an accumulator-based 3-weight test pattern generation scheme is presented; the proposed scheme generates set of patterns with weights 0, 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of BIST pattern generation, as well. Comparisons with previously presented schemes indicate that the proposed scheme compares favorably with respect to the required hardware.

INTRODUCTION:

The basic idea of Pseudorandom built-in self-test (BIST) generators is to generate test patterns on-chip and also compact the test responses of the circuit under test (CUT) on chip. The arsenal pseudorandom generators includes LFSR(linear feedback shift registers),cellular automata and accumulators driven by a constant value. For complicated circuits a large number of random patterns have to be generated.

Testing by random patterns has many advantages compared to other testing methods, for instance the self-test capability, less computing time and the high coverage of parametric faults. Hence Weighted Pseudorandom techniques have been established with a biasing inputs of either ‘0’ or ‘1’.usually weighted random pattern generation technique that rely on a single weight assignment fail to achieve complete fault coverage using number of test patterns even though the weights are suitable for most of the faults. To detect faults with these weight assignments some faults require long test sequences to be detected if they do not match their and propagation requirements. Multiple weight assingments have been proposed for different faults require different biases of the input combinations applied to the circuit to ensure that a relatively small number of patterns can detect all faults. Approaches to derive weight assignments for a given deterministic tests are efficient as they allow complete fault coverage with small number a test pattern.

Hardware Implementation cost is minimized by multiple weight assignments by using the weights as 0, 1, and 0.5.This approach boils down to keeping some outputs of the generator steady(0 or 1) other value changes as 0.5 i.e. Pseudorandom. Therefore this reduces the hardware overhead and the power consumption as some of the circuit under test (CUT) inputs remains steady as 0 or 1 during specific test session.

The basic idea of ABIST (arithmetic BIST) is to utilize accumulators for built in testing by the compression of CUT responses and has resulted in low hardware overhead and low impact on the circuit normal operating speed. It was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern can have acceptable pseudorandom characteristics if the input pattern is properly selected. Modules containing hard to detect faults may require extra test hardware either by inserting test points into the logic or by storing extra deterministic test patterns.

The Accumulator based test pattern generation have been proposed to test patterns having one of three weights 0, 1 and 0.5 can be utilized to majorly reduce the test application time. But the scheme possesses three major drawbacks 1)it increases delay as it effects the normal operating speed of the adder. 2) it can be utilized only in the case that the adder of the accumulator is a ripple carry adder 3)) It requires redesigning the accumulator, requires redesign of the core of the data path, it is not used in current BIST scheme.

The proposed Accumulator-based 3-weight generation scheme overcome the above drawbacks . Moreover 1)it does not affect the operation speed of the adder 2)do not impose any requirement about the redesign of the adder 3)it does not require any modification of the adder.

ACCUMULATOR BASED 3-WEIGHT PATTERN GENERATION:

Consider the test set for the C17 ISCAS benchmark given in table 1 to illustrate the idea of an accumulator based 3-weight pattern generation. Hence According to the proposed scheme a typical weight assignment procedure involves separating the test set into two subsets S1 and S2 as follows: S1={T1,T4} and S2={T2,T3}.

The corresponding weight assignment for these subsets is W(S1)={-,-,1,- ,1} and W(S2)={-,-,0,1,0},where "–"denotes a weight assignment of 0.5. A "1" indicates that the input is forced by logic 1 value and a "0" indicates that the input is forced by logic 0 value. In the first subsets (S1) ,inputs A[2] and A[0] are constantly driven by logic "1" while the inputs A[4],A[3] and A[1] are pseudo randomly generated value of weight "0.5".Likewise in the second subsets(S2),inputs A[2] and A[0] are constantly driven by logic "0" while the inputs A[1] is driven by "1"and inputs A[4] and A[3] are pseudo randomly generated value of weight "0".

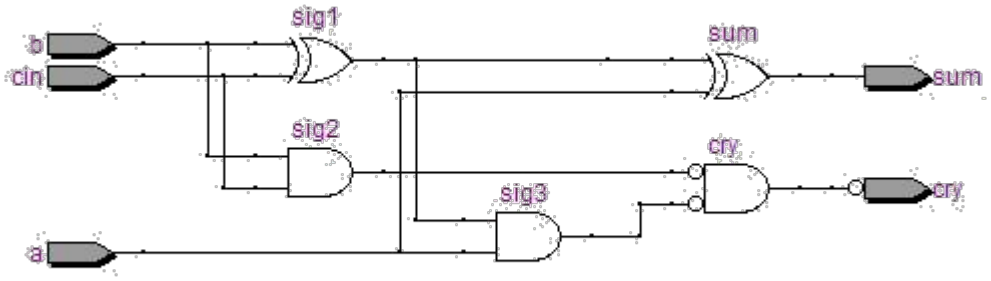


Figure 1: Full Adder Circuit

#	Cin	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	**0**	0	1	1	**0**	$C_{out} = C_{in}$
3	**0**	1	0	1	**0**	$C_{out} = C_{in}$
4	0	1	1	0	1	
5	1	0	0	1	0	
6	**1**	0	1	0	**1**	$C_{out} = C_{in}$
7	**1**	1	0	0	**1**	$C_{out} = C_{in}$
8	1	1	1	1	1	

FIG 2: Truth Table of Full Adder

The above results, configures the accumulator to meet the following conditions : 1)an accumulator output can be constantly driven by either logic “1” or ”0” and, 2)an accumulator cell with its output constantly driven to “1” or ”0” which allows the carry input to its carry output unchanged. This condition later requires to effectively generate the pseudorandom patterns in the accumulator outputs whose weight assignment is “-”.

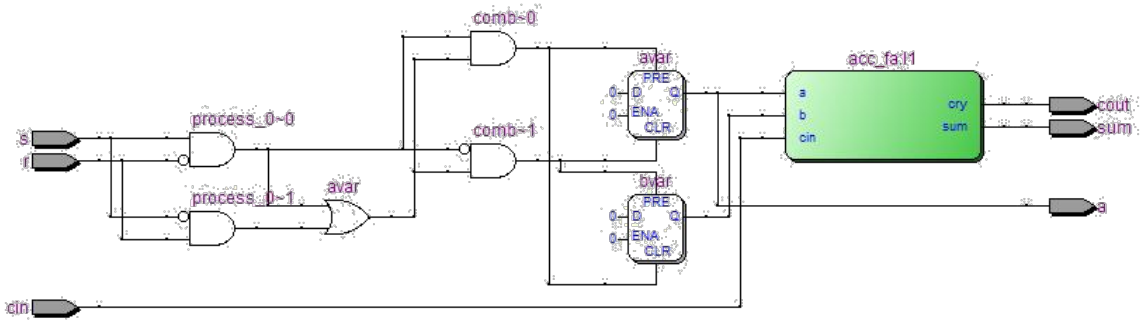
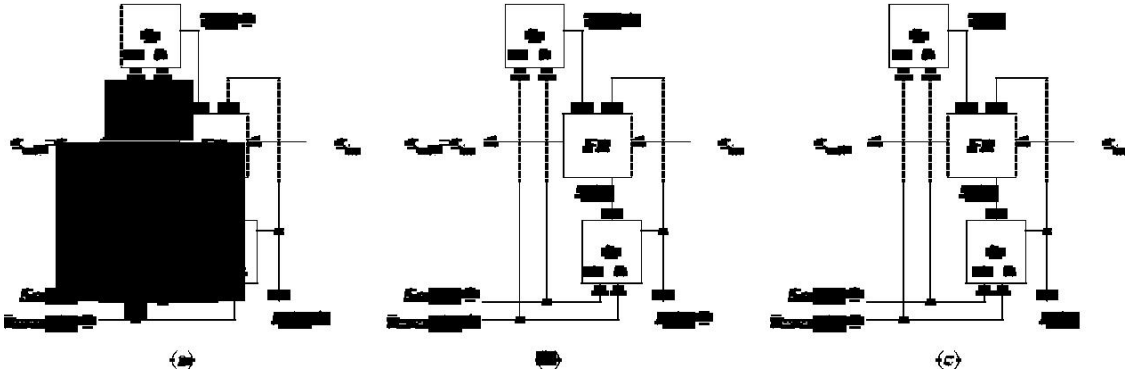


FIG 3: Accumulator cell

The implementation of the Accumulator 3-weight pattern generation is based on the accumulator cell shown in FIG3 which consists of a Full Adder (FA) cell and a D-type flip flop with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs.

DESIGN METHODOLOGY:

The implementation result of the weighted pattern generation scheme is based on the full adder truth table. We observe from the table(FIG 2) for the lines #2,#3,#6 and #7,Cout=cin. Hence to transfer the carry input to the carry output it is sufficient to set A[i]=NOT(B[i]).



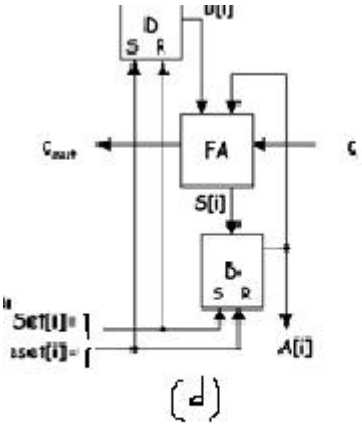


FIG 4: Configuration of the accumulator cell

The implementation of the proposed weighted pattern generation scheme is based on the accumulator cell presented in FIG 3 that consists of a full adder (FA) and a flip flop(D-Type) with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs. For this accumulator cell one out of four configurations can be utilized.

On referring Fig 4(a), the configuration that drives the CUT inputs when A[i] =1 is required. Set[i] =1 and Reset[i]=0and hence A[i] =1 and B[i] =0.Thus the output is equal to 1 and Cin value transfers to Cout. In Fig 4(b), the configuration that drives the CUT inputs when A[i]=0 is required. Set[i]=0 and Reset[i]=1and hence A[i]=0 and b[i]=1.Thus the output is equal to 0 and Cin value is transferred to Cout.

In Fig 4(c)& Fig 4(d), the configuration that drives the DUT inputs when A[i] = "-" is required. Set[i]=0 and Reset[i]=0,set[i]=1 and Reset[i]=1.The D input of Flip flop of register B is driven by either 1 or 0,depending on the value that will be added to the accumulator inputs in order to generate random patterns to the inputs of the CUT.

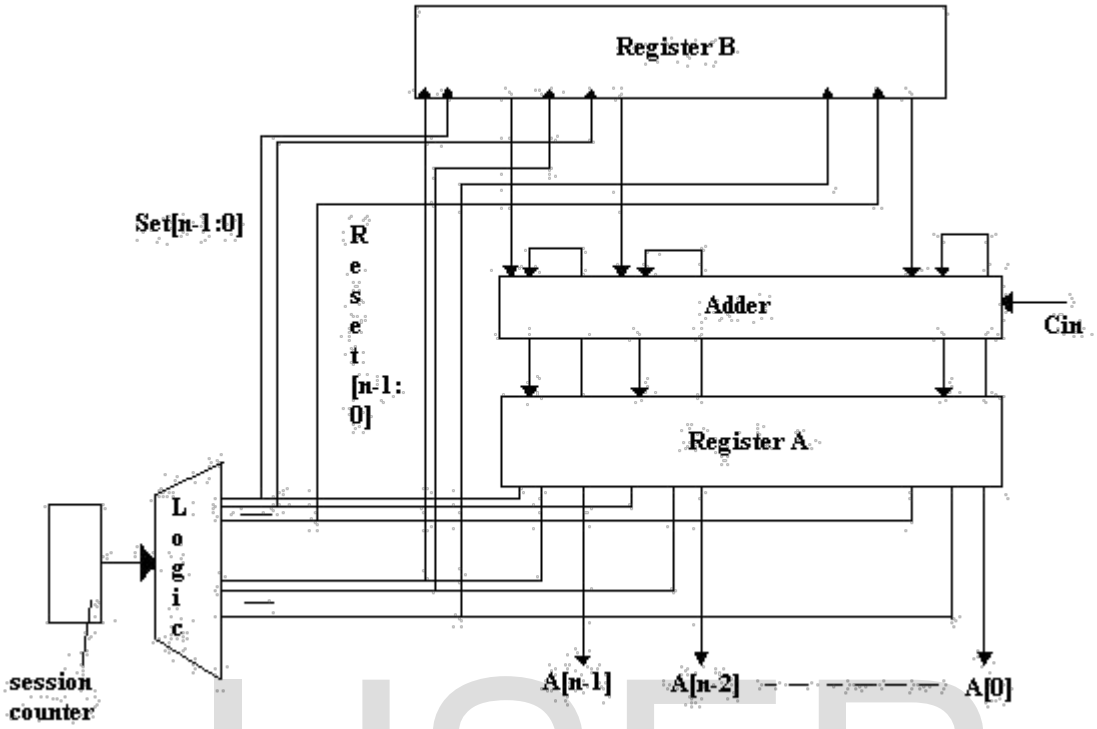
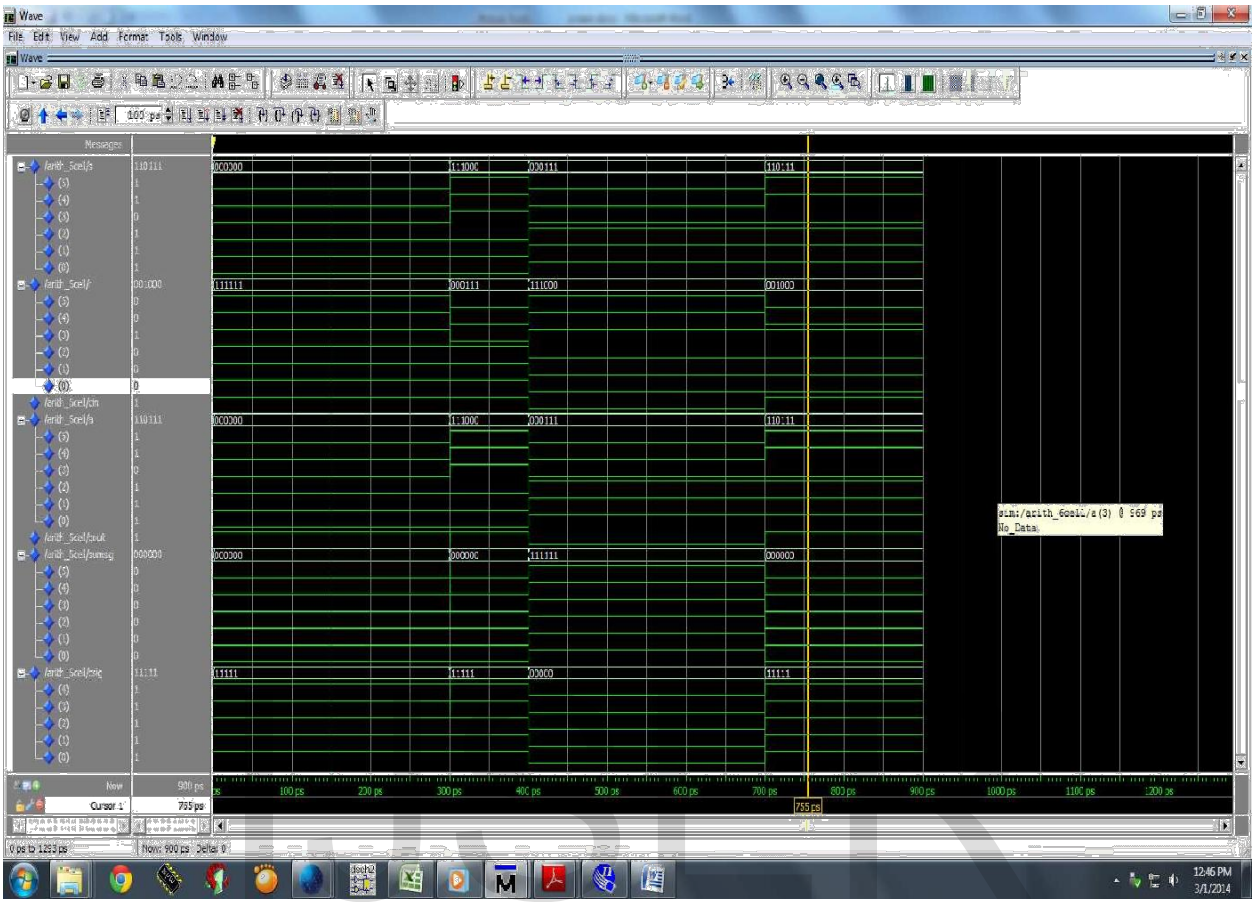


FIG 5: Proposed scheme

The Fig 5 represents the general configuration of the proposed scheme. The logic module provides that set [n-1:0] and reset [n-1:0] signals that drive the Sand R inputs of the register A and register B inputs. The signals that drive the S-inputs of the flip flops of register A, also drive the R inputs of the flip flops of register B and vice versa.

RESULT AND DISCUSSION

Implementation results have been done by using Xilinx software. Apart from the inverted inputs,) the coding is coded in such a way that ,for the input A(i)="-" (either set[i]=0,reset[i]=0or set[i]=1,reset[i]=1) the output produced would be the same as the previous output generated in the pattern, which is visible in the below output. The output generated for all random patterns is shown in the output snapshot for reference.



CONCLUSION:

This paper is presents an accumulator-based 3-weight(0, 0.5, and 1) test-per-clock generation scheme, which can be utilized to efficiently generate weighted patterns without altering the structure of the full adder. Accumulator-based 3-weight pattern generation technique lowers the hardware overhead of using the proposed scheme. Also no redesign of the accumulator is imposed, thus resulting in reduction in test application time. Comparing with the previous papers which uses weighted pattern generation technique ,this weighted pattern generation with accumulator covers all the patterns and the test time is also less. In addition this paper provides the output for all random pattern of inputs to the accumulator cell. There is 100% fault coverage without reuse of the external hardware and therefore it results in significant decrease in hardware overhead.

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